FIG. 1

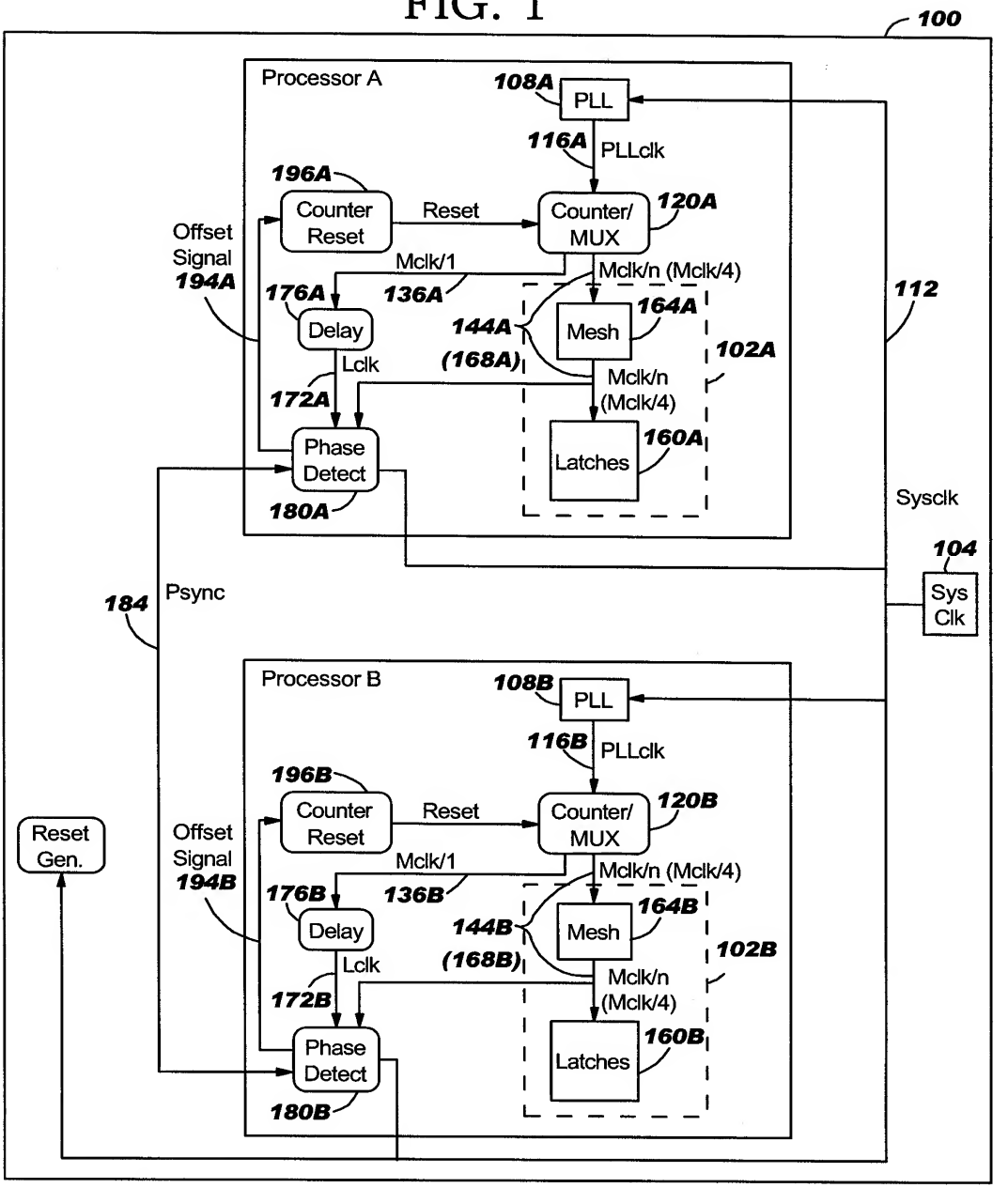

100
Processor A
108A
PLL
116A
PLLclk
196A
Counter Reset
Reset
Counter/ MUX
120A
Offset Signal
194A
Mclk/1
Mclk/n (Mclk/4)
176A
136A
112
Delay
144A
Mesh
164A
(168A)
102A
Lclk
Mclk/n (Mclk/4)
172A
Phase Detect
Latches
160A
180A
Sysclk
104
Sys Clk
184
Psync
Processor B
108B
PLL
116B
PLLclk
196B
Counter Reset
Reset
Counter/ MUX
120B
Reset Gen.
Offset Signal
194B
Mclk/1
Mclk/n (Mclk/4)
176B
136B
Delay
144B
Mesh
164B
(168B)
102B
Lclk
Mclk/n (Mclk/4)
172B
Phase Detect
Latches
160B
180B

FIG. 2A

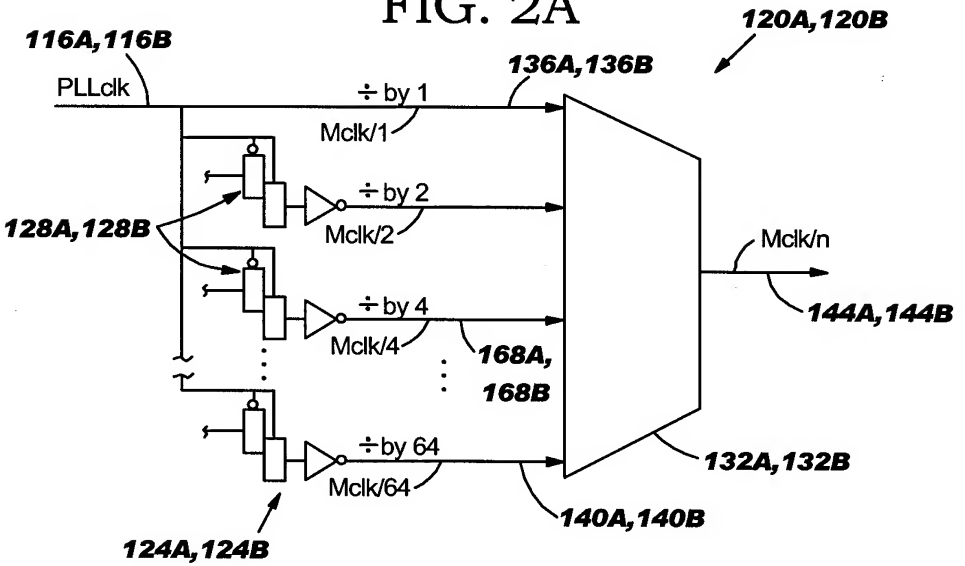

116A,116B
PLLclk
÷ by 1
Mclk/1
120A,120B
136A,136B
÷ by 2
Mclk/2
128A,128B
Mclk/n
144A,144B
÷ by 4
Mclk/4
168A,
168B
÷by 64
Mclk/64
132A,132B
140A,140B
124A,124B

FIG. 2B

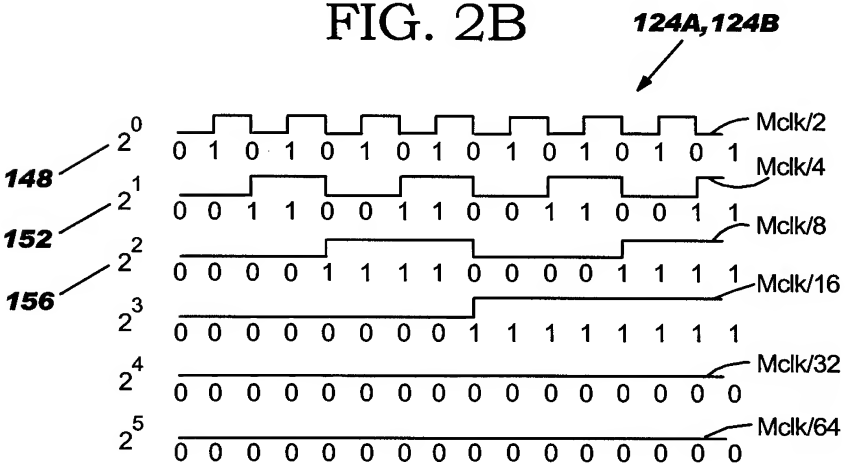

124A,124B
148
152
156
$2^0$
$2^1$
$2^2$
$2^3$
$2^4$
$2^5$
0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1
0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1
0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1
0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Mclk/2
Mclk/4
Mclk/8
Mclk/16
Mclk/32
Mclk/64

FIG. 3

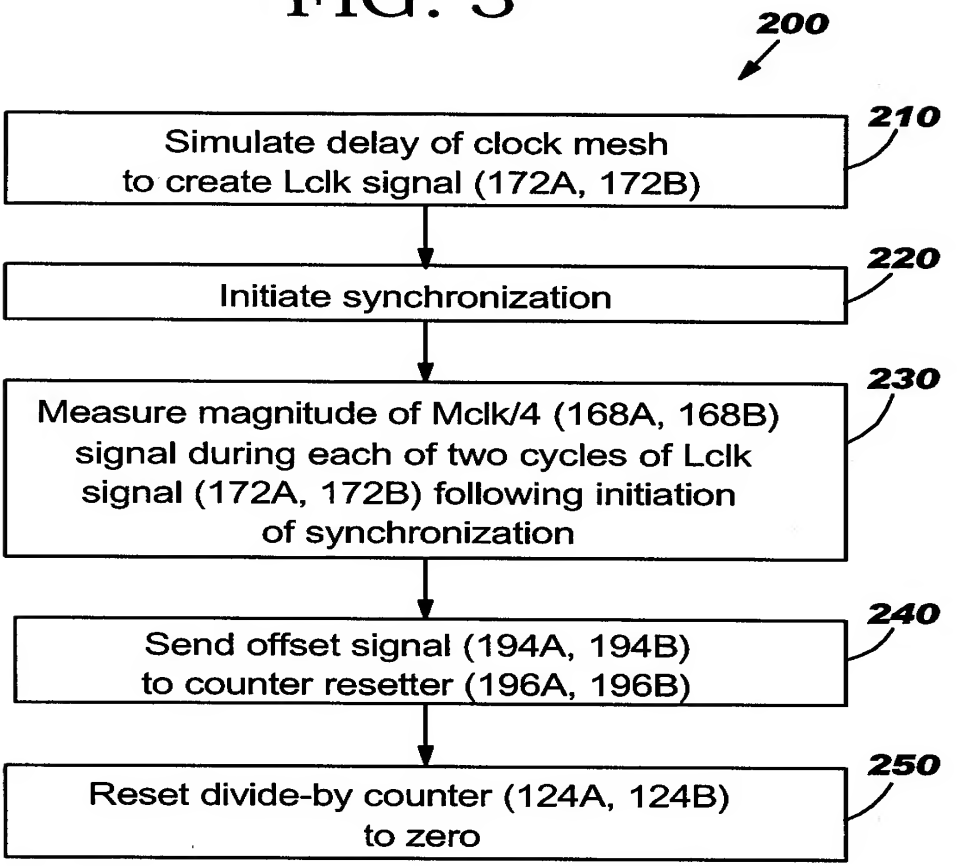
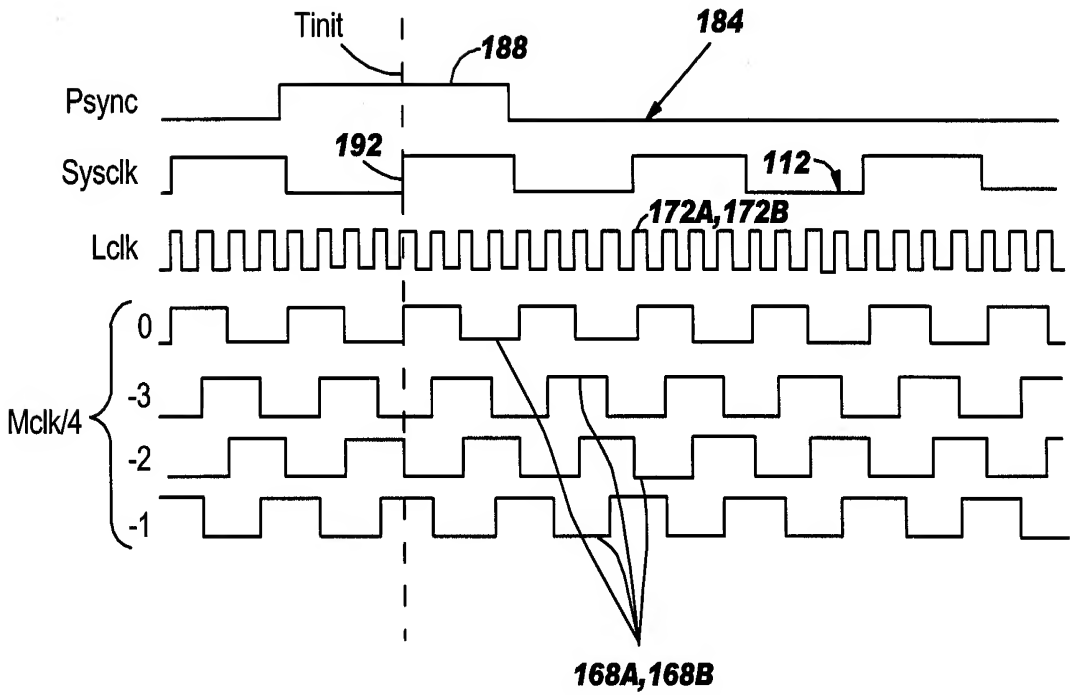

200
Simulate delay of clock mesh to create Lclk signal (172A, 172B)
210
Initiate synchronization
220
Measure magnitude of Mclk/4 (168A, 168B) signal during each of two cycles of Lclk signal (172A, 172B) following initiation of synchronization
230
Send offset signal (194A, 194B) to counter resetter (196A, 196B)
240
Reset divide-by counter (124A, 124B) to zero
250

FIG. 4


Tinit
188
184
Psync
192
Sysclk
112
172A,172B
Lclk
0
-3
-2
-1
Mclk/4
168A,168B